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Docket No. 501.42822X00
Serial No. 10/618,748
Office Action dated January 11, 2006**REMARKS**

By the present Amendment, claims 10 and 11 have been amended. Claims 13 and 14 are newly presented for consideration. Accordingly, claims 1, 2, and 8-14 are now pending in the application. Claims 1, 10, and 11 are independent.

In the Office Action of January 11, 2006, claims 1-3 and 8-12 were rejected under 35 USC §103(a) as being unpatentable over U.S. Patent No. 5,949,502 issued to Matsunaga, et al. ("Matsunaga") in view of U.S. Patent No. 5,914,763 issued to Fujii, et al. ("Fujii") and further in view of U.S. Patent No. 6,633,359 issued to Zhang, et al. ("Zhang"). These rejections are respectfully traversed.

In rejecting the claims, the Office Action alleges that Matsunaga discloses a conventional liquid crystal display device that has two transparent insulating substrates that enclose a first layer of a liquid material, a plurality of gate lines and drain lines that define pixel regions in which switching elements and transparent pixel electrodes are formed. The Office Action further alleges that Matsunaga discloses individual groups and individual gate line groups that extend into the periphery of the transparent insulating substrate to constitute external terminals which are connected with video drive circuits and gate scanning circuits.

The Office Action admits that Matsunaga does not explicitly specify that the first gate connecting lines and the second gate connecting lines are stacked in a thickness direction of the first substrate. Fujii is relied upon for disclosing a liquid crystal display with connection electrodes and leadout wirings that are arranged on sides of two substrates in a liquid crystal display device. In particular, the Office Action notes that the two substrates containing the connection electrodes and leadout wirings are stacked together such that the connection electrodes and leadout wirings are mutually stacked with respect to each other. The Office Action goes on

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to admit that Matsunaga does not explicitly specify the stacking of first and second gate connecting lines, or first and second insulating layer relationship as set forth in the claimed invention. Zhang is relied upon for "generally disclosing" a liquid crystal display wherein first and second signal lines are stacked with first and second insulating films. Applicants respectfully disagree.

At the outset, Applicants note that the Office Action has again failed to address all the features recited in the claimed invention, consequently, failing to make a *prima facie* case of obviousness. According to the Federal Circuit and the M.P.E.P., a *prima facie* case of obviousness requires that three basic criteria be met. First, there must be some suggestion or motivation in the primary reference to modify, combine, or seek out the teachings of a secondary reference. Second, there must be a realistic expectation of success from combining the two references. Finally, the prior art references must clearly teach or suggest all the claim limitations. See M.P.E.P. §706.02(j). The Federal Circuit has consistently supported the requirements of the M.P.E.P. in stating, for example, that "[i]n proceedings before the Patent and Trademark Office, the Examiner bears the burden of establishing a *prima facie* case of obviousness based upon the prior art." In re Fritch, 972 F.2d 1260, 23 USPQ 2d 1780 (Fed. Cir. 1992).

In the decision of In re Fine, 5 USPQ 2d 1596 (Fed. Cir. 1988), the court pointed out that the PTO has the burden under '103 to establish a *prima facie* case of obviousness and can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. As noted by the court, whether a particular combination might be "obvious to try" is not a

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legitimate test of patentability and obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. As further noted by the court, one cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. Furthermore, such requirements have been clarified in the decision of In re Lee, 61 USPQ 2d 1430 (Fed. Cir. 2002) wherein the court in reversing an obviousness rejection indicated that deficiencies of the cited references cannot be remedied with conclusions about what is "basic knowledge" or "common knowledge".

The Office Action admits that Matsunaga does not disclose the first gate connecting lines and the second gate connecting lines being stacked in a thickness direction of the first substrate. This feature, however, is never discussed with respect to the remaining references. The Office Action appears to misconstrue the teachings of Fujii in an attempt to address this limitation. Specifically, the Office Action indicates that Fujii discloses two substrates that are stacked together. See page 4, last paragraph of January 11, 2006 Office Action. Since Fujii discloses stacking of two different substrates containing first gate connecting lines and second gate connecting lines, respectively, it would appear that Fujii teaches away from the claimed invention. It is not clear how Fujii can possibly be construed as disclosing the claimed feature of first gate connecting lines and second gate connecting lines being stacked in a thickness direction of the first substrate as recited in the claimed invention.

Further, the Office Action appears to be completely silent on where, or how, Zhang discloses this particular feature. Zhang appears to disclose first and second signal lines formed in a first substrate. These signal lines, however, are not formed

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in the peripheral area. Rather, the signal lines are formed in the pixel area. See Figs. 3A and 4A. Further, Zhang discloses first signal lines that are connected to each other to form continuous signal lines in the column direction. See column 2, lines 35-38. In contrast, the first gate connecting lines of the claimed invention are not connected to the second gate connecting lines because they are insulated from each other by the first insulating film.

The applied references simply fail to provide any disclosure or suggestion for various features recited in independent claim 1, including at least "the first gate connecting lines and second gate connecting lines are stacked in a thickness direction of the first substrate."

It is therefore respectfully submitted that independent claim 1 is allowable over the art of record.

Claims 2, 8, and 9 depend from independent claim 1, and are therefore believed allowable for at least the reasons set forth above with respect to independent claim 1. In addition, these claims each introduce novel elements that independently render them patentable over the art of record.

Independent claim 10 defines a liquid crystal display device that comprises, in part:

the first gate connecting lines and the second gate connecting lines are stacked in a thickness direction of the first substrate, and

one of the first gate connecting lines is disposed between the two second gate connecting lines which are adjacent one another when viewed in plan view.

At least one feature of independent claim 10 provides for the first gate connecting lines to be disposed between two second gate connecting lines which are adjacent to one another when viewed in a plan view. As previously discussed with

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respect to independent claim 1, Matsunaga, Fujii, and Zhang fail to disclose first gate connecting lines and second gate connecting lines that are stacked in a thickness direction of a first substrate. Additionally, the art of record does not appear to disclose or suggest a liquid crystal display device wherein:

"one of the first gate connecting lines is disposed between the two second gate connecting lines which are adjacent one another when viewed in plan view."

Claim 13 depends from independent claim 10, and is therefore believed allowable for at least the reasons set forth above with respect to independent claim 10. In addition, claim 13 introduces novel elements that independently render it patentable over the art of record.

It is therefore respectfully submitted that independent claim 10 is allowable over the art of record.

Independent claim 11 defines a liquid crystal display device that comprises:

a first substrate, a second substrate, a third substrate, a fourth substrate, a first liquid crystal layer between the first substrate and the second substrate, and a second liquid crystal layer between the third substrate and the fourth substrate, wherein
the first substrate has a first pixel area, a first peripheral area, first gate connecting lines, and second gate connecting lines,
the third substrate has a second pixel area and a second peripheral area,
the first pixel area has first pixel electrodes, first gate lines, and first drain lines,
the first peripheral area surrounds the first pixel area,
the second pixel area has second pixel electrodes, second gate lines, and second drain lines,
the second peripheral area surrounds the second pixel area,
the first gate connecting lines and the second gate connecting lines are disposed in the first peripheral area,
the respective first gate connecting lines electrically connect the first gate lines to a liquid crystal driving circuit,
the respective second gate connecting lines electrically connect the second gate lines to the liquid crystal driving circuit,
and

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the first gate connecting lines and the second gate connecting lines are stacked in a thickness direction of the first substrate.

According to independent claim 11, the liquid crystal display device comprises a first substrate, a second substrate, a third substrate, a fourth substrate, a first liquid crystal layer between the first substrate and the second substrate, and a second liquid crystal layer between the third substrate and the fourth substrate. The first substrate has a first pixel area, a first peripheral area, first gate connecting lines, and second gate connecting lines. The third substrate has a second pixel area and a second peripheral area. Additionally, the first gate connecting and the second gate connecting lines are stacked in a thickness direction of the first substrate. This particular combination of features and elements does not appear to be disclosed by the art of record taken individually or in combination.

It is therefore respectfully submitted that independent claim 11 is allowable over the art of record.

Claims 12 and 14 depend from claim 11, and are therefore believed allowable for at least the reasons set forth above with respect to independent claim 11. In addition, these claims introduce novel elements that independently render them patentable over the art of record.

For the reasons stated above, it is respectfully submitted that all of the pending claims are now in condition for allowance. Therefore, the issuance of a Notice of Allowance is believed in order, and courteously solicited.


If the Examiner believes that there are any matters which can be resolved by way of either a personal or telephone interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

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AUTHORIZATION

Applicants request any shortage or excess in fees in connection with the filing of this paper, including extension of time fees, and for which no other form of payment is offered, be charged or credited to Deposit Account No. 01-2135 (Case: 501.42822X00).

Respectfully submitted,
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